

DRAM BIT LINES

ABSTRACT OF THE DISCLOSURE

A method for manufacturing a DRAM cell including two active word lines having a drain region and distinct source regions, including, after the forming of insulated conductive lines, the steps of: depositing a first, then a second selectively etchable insulating layers; etching the second insulating layer to only maintain it above conductive lines; depositing and leveling a third insulating layer selectively etchable with respect to at least the second insulating layer; opening the first and third insulating layers to expose the drain region and an insulating trench; filling the previously-formed opening with a conductive material; polishing the entire structure; and depositing a fourth insulating layer, selectively etchable with respect to the third insulating layer.

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